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I hereby certify that this correspondence for Application No. 10/728,348 is being electronically transmitted to Technology Center 2138, via EFS-WEB, on December 7, 2006.

/Scott A. Stinebruner/ December 7, 2006
Scott A. Stinebruner, Reg. No. 38,323 Date

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Todd Michael Burdine et al.	Art Unit:	2138
Application No.:	10/728,348	Examiner:	Cynthia H. Britt
Filed:	December 4, 2003		
For:	ABIST-ASSISTED DETECTION OF SCAN CHAIN DEFECTS		

RESPONSE AFTER NON-FINAL REJECTION

Mail Stop AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This paper is submitted in reply to the Office Action dated September 7, 2006, within the three-month period for response. Reconsideration and allowance of all pending claims are respectfully requested.

In the subject Office Action, claims 1, 3-4, 6-8, 10-11 and 13-17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,308,290 to Forlenza et al. in view of U.S. Patent Application Publication No. 2002/0125907 by Kurtulik et al. The Examiner did indicate, however, that claims 2, 5, 9, 12 and 19-20 were directed to patentable subject matter.

Applicants thank the Examiner for the finding of the allowability of claims 2, 5, 9, 12 and 19-20. Nonetheless, Applicants continue to traverse the Examiner's rejections of the remaining claims to the extent that they are maintained.

Turning first to the rejection of claim 1, this claim generally recites a method of detecting a defect in a scan chain, which includes applying a plurality of pattern sets to a scan chain using an array built-in self-test (ABIST) circuit coupled to the scan chain,

collecting, from the scan chain, scan out data generated as a result of the application of the plurality of pattern sets to the scan chain, and using the collected scan out data to identify a defective latch in the scan chain.

As such, the claim effectively recites the identification of a defective latch in a scan chain based upon scan out data collected as a result of the application of test patterns to the scan chain by an ABIST circuit.

In the present Office Action, the Examiner acknowledges that Forlenza does not disclose a scan chain that is coupled to an ABIST circuit. However, the Examiner now relies on Kurtulik for allegedly disclosing an "ABIST coupled to a scan chain for testing," citing Figs. 5-7 of the reference (Office Action, page 4).

It is important to note, however, that claim 1 does not merely recite an ABIST circuit coupled to a scan chain. The ABIST circuit recited in claim 1 is not only coupled to a scan chain, but the ABIST circuit is the entity that generates the test patterns that are applied to the scan chain, and thus initiates the generation of the scan out data that is used to identify a defective latch.

Kurtulik, and in particular Figs. 5-7 thereof, merely discloses the conventional use of an ABIST engine for testing arrays in a chip. These figures, which are discussed in detail in paragraphs [0037]-[0043], disclose an ABIST engine that is in fact coupled to one or more scan chains. In each instance, however, the scan chains to which the ABIST engine is coupled are used either to provide input test data to an array during testing of the array, or to capture output data from the array that is generated during testing. Put another way, the scan chains are used in their conventional manner to test arrays, and the testing protocol that an ABIST engine undergoes in connection with testing arrays presumes that these scan chains are not defective.

In the event that a latch in one of the scan chains was defective, the Kurtulik ABIST engine would not be able to correctly test any arrays; however, there is no disclosure or suggestion in the reference that a defective latch may be detected using an ABIST engine. This is not particularly surprising because Kurtulik does not address the issue of testing the scan chains themselves for defects. Kurtulik has no concern for defective scan chains, and as a result, Applicants submit that Kurtulik cannot be relied

upon to not disclose or suggest that an ABIST circuit could be used in connection with identifying defective latches in a scan chain.

As the Examiner has acknowledged, Forlenza does not disclose or suggest an ABIST circuit coupled to a scan chain. Consequently, Forlenza also cannot be relied upon to disclose or suggest the use of an ABIST circuit to apply test patterns to a scan chain for the purpose of identifying a defective latch in the scan chain. Likewise, Kurtulik, which does not address defective scan chains, also cannot be relied upon to suggest the identification of defective latches in a scan chain using an ABIST circuit. Therefore, neither reference discloses or suggests that an ABIST circuit could be used to generate the test patterns from which a defective latch in a scan chain is identified.

The Examiner has provided no other objective evidence of a suggestion in the art to use an ABIST circuit for this particular purpose. Accordingly, Applicants submit that the Examiner has failed to establish a *prima facie* case of obviousness with respect to claim 1. Lacking any such evidence, the rejection is necessarily and improperly reliant on hindsight, and should be withdrawn.

The Examiner does argue in support of the rejection that ABIST is merely a "design choice" and a specific type of BIST, citing col. 6, lines 29-33 of Forlenza. Applicants strenuously traverse this argument, however, as there is no suggestion within the reference, or anywhere else in the prior art, of the specific application of ABIST for the purpose of applying test patterns to a scan chain to identify a defective latch. Given that BIST can incorporate other types of test circuitry, e.g., LBIST, it is only through the benefit of hindsight that the Examiner could reason that the general disclosure of BIST suggests the use of ABIST in this specific application.

It is also important to note that the teachings of references must be considered as a whole, and in the case of Forlenza, the BIST circuitry is specifically used to store test patterns on-chip for the purpose of eliminating the need to load test patterns from off-chip when performing look ahead scan chain diagnostics. Given that ABIST circuits *generate* test patterns, rather than retrieve test patterns from any form of memory storage, Applicants respectfully submit that Forlenza, and in particular, the disclosure of BIST circuitry that incorporates memory storage for storing test patterns, does not suggest that

ABIST is a suitable alternative for the disclosed BIST circuit. Indeed, given that the disclosed BIST circuit stores test patterns, Applicants respectfully submit that Forlenza specifically teaches away from the use of an ABIST circuit to generate pattern sets, as is required by claim 1.

Applicants have also previously noted the unique and unexpected advantage of using an ABIST circuit over the BIST circuit disclosed in Forlenza, given the elimination of the substantial storage requirements that the Forlenza BIST circuit would require to store the appropriate test patterns.

The Examiner also presumably argues in support of the rejection that the latches or flip flops in a scan chain are memory elements, and that ABIST circuits are used to test memory elements in an array. This argument, however, discounts the unique nature of a scan chain, which is recognized by one of ordinary skill in the art as a separate circuit component from a memory array that is conventionally tested by an ABIST circuit. Indeed, scan chains are regularly used for the purpose of assisting in the testing of a memory array, as exemplified by Kurtulik. Once again, it is only through the benefit of hindsight that one would be motivated to use an ABIST circuit to apply test patterns to a scan chain for the purpose of identifying a defective latch in that scan chain.

Applicants therefore respectfully submit that claim 1 is non-obvious over Forlenza and Kurtulik, as well as the other prior art of record. Reconsideration and allowance of claim 1, and of claims 2-7 which depend therefrom, are therefore respectfully requested.

Next, with respect to independent claims 8 and 17, each of these claims recites, in part, the concept of "collecting, from [a] scan chain, scan out data generated as a result of an application of a plurality of pattern sets to the scan chain by an array built-in self-test (ABIST) circuit" for the purpose of identifying a defective latch in the scan chain. As discussed above in connection with claim 1, neither Forlenza nor Kurtulik, alone or in combination, discloses or suggests the concept of applying pattern sets to a scan chain using an ABIST circuit for the purpose of identifying a defective latch in the scan chain, and the use of an ABIST circuit to perform such a function represents more than merely a design choice. Accordingly, claims 8 and 17 are non-obvious over Forlenza and Kurtulik for the same reasons presented above for claim 1. Reconsideration and allowance of

claims 8 and 17, and of claims 9-16 and 18 which depend therefrom, are therefore respectfully requested.

Next, with respect to the various rejected dependent claims, Applicants traverse the Examiner's rejections based upon the dependency of these claims on the aforementioned independent claims. A number of these claims, however, recite additional features that further distinguish these claims from the prior art of record, and warrant additional mention.

For example, claims 7 and 14 recite the concept of reconfiguring a scan chain prior to collecting the scan out data. The passage cited against these claims by the Examiner, at col. 4, lines 30-38, discloses only passing 0 and 1 patterns through a scan chain, and is completely silent with respect to reconfiguring a scan chain.

Accordingly, Applicants submit that the Examiner has failed to establish a *prima facie* case of obviousness as to claims 7 and 14. Reconsideration and allowance of these claims are therefore respectfully requested.

In summary, Applicants respectfully submit that all pending claims are novel and non-obvious over the prior art of record. Reconsideration and allowance of all pending claims are therefore respectfully requested. If the Examiner has any questions regarding the foregoing, or which might otherwise further this case onto allowance, the Examiner may contact the undersigned at (513) 241-2324. Moreover, if any other charges or credits are necessary to complete this communication, please apply them to Deposit Account 23-3000.

Respectfully submitted,

December 7, 2006
Date

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